REMARKS

This amendment is being filed as a response to the Office Action of February 5, 2008. Reconsideration is respectfully requested in view of these clarifying amendments and remarks.

Rejections under 35 USC § 103(a)

Claims 1-5 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Higashi (US Patent No. 6,873,332), in view of Nishikawa (U.S. Patent No. 5,021,950). This rejection is respectfully traversed. Applicants respectfully request reconsideration of these rejections in light of the amendments and arguments contained herein.

In the spirit of expediting the prosecution of the present application, Applicant has amended claim 1 to further distinguish Applicant's claim language from the above references, as follows:

"requesting by a processor access to a module in a display controller;

processing continuously in the processor until notification [[by]]that the module in the display controller is available; [[,]]

sending by ~~wherein~~ a multiplexer in the display controller ~~sends a first~~ an available signal to a pin in the processor, the pin in the processor having a dual function, wherein one of the dual functions is to notify the processor that ~~when~~ the module is available; and

accessing by the processor the module in the display controller after ~~receiving~~ sending the ~~first~~ available signal via the pin."

There is no suggestion in Higashi or Nishikawa of a **dual function pin**. Additionally, module ROM 105, as seen in Figure 1 of Higashi, is not part of the display controller, as claimed by Applicants. Multiplexer 61 of Nishikawa is not part of the display controller either. Multiplexer 61 is part of Stop Control Block 33 as seen in Figure 2, and Stop Control Block 33 is part of processor module 11, as seen in Figure 1. Thus, a processor module that "performs data processing" (Col. 2, line 56) is not a display controller, as claimed by Applicants.

Additionally, with respect to the motivation of combining Higashi and Nishikawa, the Office has asserted that the combination "would have provided the means for increasing processing capabilities by use of a waiting signal with the used (sic) of multiplexers and arbitration blocks to allow the a more advanced and a continuous processing of data to between processing and the system to eliminate wasted time processing only during the availability of the system." This is an improper motivation on its face since it does not make any sense. Applicants respectfully request that the Office clearly explains the motivation to combine, and more specifically how "to eliminate wasted time processing only during the availability of the system." Is there any other way of processing than when the system is available? How will wasted time be eliminated?

Claims 18-24 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikawa, in view of Kirmuss (U.S. Publication No. 2003/0081934 A1). This rejection is respectfully traversed. Applicants respectfully request reconsideration of these rejections in light of the amendments and arguments contained herein.

In the spirit of expediting the prosecution of the present application, Applicant has amended independent claim 18 to further distinguish Applicant's claim language from the above references, as follows:

"a plurality of ~~first~~ modules internal to the controller~~, the plurality of first modules being capable of accessing a plurality of second modules external to the controller~~;

a combinatorial multiplexer that selects one of the modules in the plurality of modules;

[[a]] an input/output (I/O) multiplexer ~~coupled to the~~ selecting either a wait signal or a busy signal received from the combinatorial multiplexer, the busy signal indicating whether the selected module by the combinatorial multiplexer is available ~~plurality of first modules via a combinatorial multiplexer, the multiplexer being capable of transmitting a second signal to a pin by selecting one of a wait signal and a busy signal in the multiplexer in response to the first signal~~; and

a connector transmitting the output of the I/O multiplexer to a pin in a processor, the pin in the processor having a dual function, wherein one of the dual

functions is to notify the processor that the module is available ~~coupled to the multiplexer and the pin, the connector being capable of transmitting the second signal to a source of the first signal."~~

Claim 18 is believed to be patentable for at least the same reasons presented for independent claim 1. Kirmuss does not teach dual function pins, therefore there is no suggestion in the references of a dual function pin, and the rejection of claim 18 is now moot.

In view of the foregoing, the Office is requested to withdraw the rejection of claims 1 and 18 under §103. The dependent claims are submitted to be patentable for at least the same reasons the independent claims are believed to be patentable. The Applicants therefore respectfully request reconsideration and allowance of the pending claims. A Notice of Allowance is respectfully requested. In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach Applicant's attorney Michael L. Gencarella (44,703) at (408) 774-6921.

Respectfully submitted,

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Date: April 15, 2008